## Abstract of the Disclosure

A non-volatile transistor memory array has individual cells with a current injector and a non-volatile memory transistor. Injector current gives rise to charged particles that can be stored in the memory transistor by tunneling. When a row of the array is activated by a word line, the active row has current injectors ready to operate if program line voltages are appropriate to cause charge storage in a memory cell, while a cell in an adjacent row be erased by charge being driven from a memory transistor. A series of conductive plates are arranged over the word line, with each plate having a pair of oppositely extending tangs, one causing programming of a cell in a first row and another causing erasing of a cell in another row.